AIDA4Edge

2nd AIDA4Edge Training School

IHP - Leibniz Institute for High Performance Microelectronics
Frankfurt (Oder), Germany

11 - 13 May 2026

Università degli Studi di Ferrara

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AIDA4Edge (Twinning for Excellence in Adaptive Edge AI) Project – Brief Overview

Artificial intelligence (AI) algorithms are currently one of the most powerful tools for solving the most challenging problems, becoming one of the leading research topics and one of the areas with the largest investment in recent years. Disruptive in nature, AI technologies have brought revolutionary changes in many areas. However, one of the main issues preventing the wider application of AI technologies is the high complexity of AI algorithms, which require very expensive and specialized hardware (servers, clouds). In this classical AI concept with complex algorithms of **Artificial Neural Networks (ANN)** running on clouds, data has to be sent over the Internet to the cloud, causing latency (preventing real-time AI-based applications) as well as issues with security and privacy. Therefore, one of the main directions of cutting-edge research in the field of AI is **bringing AI to the Edge**, which means designing AI algorithms of reduced complexity that will enable their deployment on edge devices with constrained resources in terms of memory, processing power, energy consumption and latency. This will allow AI algorithms to be executed on local hardware devices as close as possible to the physical system, thus providing a number of new AI-based applications that could fundamentally change various aspects of human life.

In brief, AIDA4Edge aims to exploit the synergy of the expertise of the advanced EU partners to provide the Faculty of Electronic Engineering, University of Niš team with necessary knowledge through comprehensive research activities. In addition, it is conceived to increase performance of the Faculty of Electronic Engineering, University of Niš in a pervasive way (enhance networking activities, raise reputation, research profile and attractiveness, strengthen research management capacities and administrative skills).

Project partners:

- Faculty of Electronic Engineering, University of Niš - project coordinator
- IHP - Leibniz Institute for High Performance Microelectronics
- University of Manchester
- University of Ferrara

https://aida4edge.elfak.rs/

2nd AIDA4Edge Training School

AIDA4Edge

“Reliable and Efficient AI Hardware Accelerators”

Technical Program

IHP - Leibniz Institute for High Performance Microelectronics
Frankfurt (Oder), Germany

11 - 13 May 2026

Monday, 11th May

9:30 – 10:30: Registration

10:30 – 10:45: Opening Session and IHP's Welcoming Address
Fabian Vargas, Marko Andjelkovic

10:45 – 11:00: AIDA4Edge Introduction
Milan Dincic, AIDA4Edge coordinator, Faculty of Electronic Engineering, University of Nis, Serbia

11:00 – 11:45: Keynote Talk 1
DFT HW Reuse for Self Health-Awareness and Fault Recovery in a Multicore CPU Subsystem
Artur Jutman, Tallinn University of Technology (TalTech), Estonia

11:45 – 12:15: Coffee-Break

12:15 – 13:00: Keynote Talk 2
Runtime-Adaptive Cross-Level Techniques for Efficient and Reliable Edge AI
Mahdi Taheri, Brandenburg University of Technology Cottbus-Senftenberg, Germany

13:00 – 14:00: Lunch

14:00 – 14:30: Lecture 1
Resistive RAM for In-Memory Computing in Extreme Environments
Emilio Perez-Bosch Quesada, IHP, Germany

14:30 – 15:00: Lecture 2
RRAM-Based Frequency-Domain Convolution Accelerator for Reliable and Energy-Efficient CNN Inference
Jianan Wen, IHP, Germany

15:00 – 15:30: Coffee-Break

15:30 – 16:00: Lecture 3
Understanding Fault Propagation in RRAM-based CIM Architectures
Andre Lucas Chinazzo, IHP, Germany

16:00 – 17:00: Project meeting

Tuesday, 12th May

10:00 – 11:00: Registration

11:00 – 11:45: Lecture 4
Exploring Hybrid Brain-Inspired Architectures and Technology Heterogeneity for High Performance AI Applications: Challenges & Solutions
Leticia Bolzani Poehls, IHP, Germany

11:45 – 12:15: Coffee-Break

12:15 – 13:00: Keynote Talk 3
EDA Agentic AI: Current Status, Challenges and Future Roadmap
Christos Sotiriou, University of Thessaly, Greece

13:00 – 14:00: Lunch

14:00 – 14:30: Lecture 5
Chip Design Using Open Source EDA and PDK – Status Update
Krzysztof Herman, IHP, Germany

14:30 – 15:00: Lecture 6
An Overview of Fault Injection Techniques for Neural Network Accelerators
Rizwan Tariq Syed, IHP, Germany

15:00 – 15:30: Coffee-Break

15:30 – 16:30: Project meeting

19:00 – 22:00: Dinner at Restaurant "Villa Casino", Slubice, Poland
(All participants should take IDs or passports due to possible border control)
Dinner is sponsored by IHP Solutions

Wednesday, 13th May

10:00 – 11:00: Registration

11:00 – 11:45: Keynote Talk 4
When Hardware Fails, Does Intelligence Survive? Faults in Neuromorphic Communication Hardware
Davide Bertozzi, University of Manchester, United Kingdom

11:45 – 12:15: Coffee-Break

12:15 – 13:00: Lecture 7
Considerations on the Mixed-Criticality Task Execution in Multicore Architecture for Real-Time Applications
Fabian Vargas, IHP, Germany

13:00 – 14:00: Lunch

14:00 – 14:30: Lecture 8
Commercialization of Academic Research Results
Anders Henriksson, IHP Solutions, Germany

14:30 – 15:00: Lecture 9
Preparing Project Proposals
Milos Krstic, IHP, Germany

15:00 – 15:30: Coffee-Break

15:30 – 16:30: Project meeting

16:30 – 17:00: Closing session

Notes:

All sessions will take place in room D1 (first floor).

Main contact:

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2nd AIDA4Edge Training School

AIDA4Edge

"Reliable and Efficient AI Hardware Accelerators"

Short Bios of the Speakers and Abstracts of the Lectures

IHP - Leibniz Institute for High Performance Microelectronics
Frankfurt (Oder), Germany

11 - 13 May 2026

Monday, 11th May

11:00 – 11:45: Keynote Talk 1

DFT HW Reuse for Self Health-Awareness and Fault Recovery in a Multicore CPU Subsystem

Artur Jutman, Tallinn University of Technology (TalTech), Estonia

Bio: Artur Jutman is a founder and Managing Director of Testonica since 2005. He got a PhD degree in computer engineering from TalTech, Estonia in 2004. He co-authored a textbook as well as over 160 peer-reviewed research papers on topics embracing embedded instrumentation, DFT, system health management as well as IC and system test in a broad sense. He is a member of the steering committees of European Test Symposium, Estonian Electronics Industries Association, and the Nordic Test Forum society. Dr. Jutman has coordinated several EU-funded research consortia, participated in organizing conferences and workshops across Europe as well as given several keynotes, invited talks and tutorials at conferences and symposia.

Abstract: As multicore CPU subsystems grow in complexity, ensuring reliable operation in the presence of defects, aging, and in-field faults has become a major challenge. While Design-for-Test (DFT) infrastructures are typically limited to production use, they offer significant untapped potential for enabling in-field self-health awareness and resilience.
This talk explores how IC-level DFT hardware - such as scan chains, monitors, checkers and other embedded instrumentation (particularly following the IEEE Std. 1687 / IJTAG) - can be reused for runtime health monitoring, fault localization, and adaptive recovery. The talk will introduce architectural concepts that integrate DFT-based observability into system-level health management, enabling real-time anomaly detection and targeted mitigation demonstrated on a satellite case study.
Focusing on multicore systems, we discuss key challenges such as distributed monitoring and coordinated recovery, and show how existing test resources can enhance robustness with minimal overhead. The talk highlights a shift toward viewing DFT as a runtime asset for building self-aware, resilient computing systems.

12:15 – 13:00: Keynote Talk 2

Runtime-Adaptive Cross-Level Techniques for Efficient and Reliable Edge AI

Mahdi Taheri, Brandenburg University of Technology Cottbus-Senftenberg, Germany

Bio: Mahdi Taheri received his B.Sc. degree in electrical engineering in 2017 and his M.SC. degree in electrical engineering in 2021. He received his Ph.D. at Tallinn University of Technology in Jan. 2025, and since then, he has been a postdoctoral researcher at BTU Cottbus and a part time researcher at TalTech. His research interests include reliability and fault tolerance design, approximate computing, neural networks, and hardware accelerators.

Abstract: With the rapid advancement of AI models and the pursuit of ever-higher accuracy, their deployment is increasingly expanding into safety-critical edge environments. However, implementing state-of-the-art models on resource-constrained devices while simultaneously ensuring efficiency and reliability has become a fundamental challenge. This talk presents a cross-level, runtime-adaptive optimization paradigm for efficient and reliable edge AI acceleration. Unlike conventional static and single-level approaches, the proposed methodology coordinates optimizations across the model, hardware architecture, and arithmetic levels, enabling input-aware computation and accelerator-specific configuration tuning. Such coordinated adaptivity unlocks efficiency–reliability trade-offs that remain unattainable through isolated optimizations, providing a practical foundation for next-generation adaptive and dependable edge AI systems.

14:00 – 14:30: Lecture 1
Resistive RAM for In-Memory Computing in Extreme Environments
Emilio Perez-Bosch Quesada, IHP, Germany

Bio: Emilio Perez-Bosch Quesada is a researcher specializing in the electrical characterization and modeling of HfO_2-based resistive random-access memory (RRAM) devices for advanced computing applications. He earned his Bachelor's degree in Telecommunication Engineering from the University of Jaén, Spain, in 2017. In 2019, he completed a double Master's degree in Telecommunication Engineering from the University of Jaén and the Technische Hochschule Mittelhessen (THM) in Germany, where he was awarded the Best Master's Thesis Award. He pursued his PhD at IHP – Leibniz Institute for High Performance Microelectronics in Frankfurt (Oder), Germany, focusing on the electrical characterization and modeling of HfO_2-based RRAM devices for neuromorphic computing. After receiving his PhD in July 2024, his research has expanded to evaluating RRAM technology under harsh environmental conditions, with the goal of enabling in-memory computing for space applications and quantum computing.

Abstract: HfO2-based RRAM devices exhibit promising electrical properties under extreme environmental conditions, making them strong candidates for radiation-hardened and cryogenically compatible electronics in space and quantum computing applications. Their inherent radiation tolerance and reliable operation at cryogenic temperatures are key advantages for implementing in-memory computing (IMC) systems in these domains. However, despite extensive research on RRAM-based IMC, their performance in harsh conditions remains largely unexplored.
In this talk, I will present recent advances from IHP's Materials Research department on the development of radiation-hardened-by-design RRAM devices, capable of operating under harsh radiation in a multilevel approach. Additionally, I will demonstrate their switching capabilities at 1.5 Kelvin, establishing a new operational benchmark for this technology. Based on experimental results, I will highlight key reliability considerations for integrating IHP's RRAM technology into larger IMC systems for space and quantum computing applications.

14:30 – 15:00: Lecture 2

RRAM-Based Frequency-Domain Convolution Accelerator for Reliable and Energy-Efficient CNN Inference

Jianan Wen, IHP, Germany

Bio: Jianan Wen received the B.Sc. degree in electrical engineering from the University of Duisburg-Essen, in 2017, and the M.Sc. degree in information technology from RWTH Aachen University, Germany, in 2020. He is currently pursuing the Ph.D. degree with the University of Potsdam. Since 2021, he has been a Researcher at the IHP-Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany. His research focuses on fault-tolerant RRAM-based systems for signal processing and AI accelerators.

Abstract: The increasing computational demands of convolutional neural networks (CNNs) have motivated the exploration of alternatives to computationally intensive spatial-domain convolutions. The convolution theorem establishes that convolution in the spatial domain can be computed by the elementwise multiplication in the frequency domain. By leveraging this property, the sequential sliding-window operations in convolutional layers can be eliminated, leading to reduced computational complexity and hardware cost. This talk surveys existing frequency-domain CNN accelerators that exploit this transformation to enhance energy efficiency. It then introduces an RRAM-based accelerator architecture that integrates the device-level advantages of RRAM crossbar arrays with the algorithmic benefits of frequency-domain convolution. The proposed design enables reliable and energy-efficient convolutional layer execution, highlighting the potential of frequency-domain operations for accelerating CNN inference.

15:30 – 16:00: Lecture 3

Understanding Fault Propagation in RRAM-based CIM Architectures

Andre Lucas Chinazzo, IHP, Germany

Bio: André Chinazzo received the B.Sc. degree in electrical engineering from the Federal University of Rio Grande do Sul, Brazil, and M.Sc. degree in Integrated Systems from TU Kaiserslautern, Germany. He is currently pursuing his Ph.D. degree at IHP, focusing on reliability-aware design of hardware accelerators for AI.

Abstract: As AI models grow, the von Neumann bottleneck severely limits performance, even in specialized hardware like systolic arrays. Computing-in-Memory (CIM) architectures offer a promising solution by processing data directly within memory arrays. However, hardware reliability remains a critical challenge. This presentation explores the fault propagation behaviors inherent in CIM systems, specifically comparing stateful and non-stateful architectures. By understanding how errors manifest in these distinct paradigms, we can design more robust, reliable AI hardware.

Tuesday, 12th May

11:00 – 11:45: Lecture 4

Exploring Hybrid Brain-Inspired Architectures and Technology Heterogeneity for High Performance AI Applications: Challenges & Solutions

Leticia Bolzani Poehls, IHP, Germany

Bio: Leticia Maria Bolzani Pöhls graduated in Computer Science at UFPel (Brazil) in 2002 and holds a master's degree in Electrical Engineering from PUCRS (Brazil) since 2004. In 2008 she obtained her Ph.D. in Computer Engineering from Politecnico di Torino (Italy). From 2010 to 2022 she was Professor at the School of Technology at PUCRS (Brazil). For her sabbatical year she joined the Chair of Integrated Digital Circuits and System Design (IDS) at RWTH Aachen University (Germany) in 2019. In 2020 she created and until 2024 led the Group of Test and Reliability of Emerging Applications at IDS. In January 2025 she joined IHP - Leibniz Institute for High Performance Microelectronics (Germany) where she is leading the Group of Neuromorphic Hardware in the Department of System Architectures. Amongst her activities in the scientific community, she works as a member of the Steering Committee of IEEE Latin American Test Symposium (LATS) as well as the working group of VLSI-SoC. In addition, she is part of the organizing committee of several conferences such as ETS, DATE, DDECS, VTS, and ITC. Finally, she received the 2021 JETTA-TTTC Best Paper Award, the IEEE LATS2022 Best Paper Award, and the HiPEAC 2023 Paper Award for her paper at the Design Automation Conference (DAC2023).

Abstract: High-performance Edge AI applications require not only the adoption of nonconventional architectures, but also the combined use of CMOS and emerging technologies. In addition, the design of disruptive brain-inspired hardware for edge AI applications poses challenges related to power consumption, quality and reliability. In more detail, the adoption of hybrid brain-inspired architectures based on the heterogeneous integration of different types of circuits, analog, digital or mixed-signal, as well as technology nodes and device technologies, pose significant challenges. Thus, a deep understanding of how to deal with the heterogeneity at circuit level assuming hybrid brain-inspired architectures and how manufacturing and time-dependent deviations impact their quality and reliability is considered mandatory. This talk presents a holistic perspective on the sources of quality and reliability issues of hybrid brain-inspired architectures that explores heterogeneity at circuit level, as well as their impact at circuit, architecture and system level. Finally, this talk summarizes strategies able to guarantee highly reliable edge AI architectures.

12:15 – 13:00: Keynote Talk 3
EDA Agentic AI: Current Status, Challenges and Future Roadmap
Christos Sotiriou, University of Thessaly, Greece

Bio: Christos P. Sotiriou is Associate Professor in the Department of Computer Science and Electrical Engineering of the University of Thessaly. He received his Ph.D. in computer science from the University of Edinburgh in 2001. He is author of over 31 journal and conference papers and holds 7 patents. He has served as Chair of the International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC) as well as other conferences and symposia. He specializes in digital circuit design, CAD tools and algorithms, and asynchronous circuit design.

Abstract: Agentic AI is rapidly moving from experimental demos to active deployment in production EDA flows. In this talk, we will present the current state of EDA Agentic AI, focusing on its current capabilities and challenges, as well as requirements for building such as flow. We will explore practical problem statements, and specifically explore the areas of (1) RTL code checking and fixing, (2) specification to automated Testbench construction for design verification, and (3) Synthesis to GDSII Agentic flow.
We will detail challenges and constraints of EDA Agentic AI, including LLM infrastructure requirements, IP and data protection and flow determinism. We will present the capabilities and challenges of NPU/CPU based SLMs (Small Language Models), which offer secure, on-premise deployment with low-cost edge devices such as laptops and edge inference servers. To leverage SLMs for architectural reasoning and complex multi-step planning we investigate and present approaches on how to bridge the SLM, LLM gap. Looking ahead, we will conclude with a specification roadmap for EDA Agentic AI flows, which address the current shortcomings into the future.

14:00 – 14:30: Lecture 5
Chip Design Using Open Source EDA and PDK – Status Update
Krzysztof Herman, IHP, Frankfurt (Oder), Germany

Bio: Krzysztof Herman - graduated from Wroclaw University of Science and Technology, Wroclaw, Poland completing his M.Sc. in Acoustics and D.Sc. in Telecommunications engineering in 2007 and 2013 respectively. During early years of his research career worked at Wroclaw University of Science and Technology investigating air coupled ultrasound arrays and beamforming techniques and participated in two polar scientific expedition to the Arctic and the Antarctic. In the period of 2015 to 2022 worked as a researcher and an academic teacher at the Department of Electrical and Electronics Engineering, University of the Bio-Bio, Concepcion, Chile. He considers himself to be one of the first "victims" of the open-source silicon movement, in which he got involved a few years ago. Currently works as a research assistant at IHP Frankfurt (Oder) developing IHP's open source PDK and handling open-source MPW submissions.

Abstract: Recent developments in the IHP SG13G2 open-source PDK have substantially improved design enablement across digital, analog, and mixed-signal domains, while the introduction of SG13CMOS5L provides a fast and cost-efficient entry point for prototyping. SG13G2 now features practical support for OpenROAD-based digital implementation flows through LibreLane, enabling streamlined RTL-to-GDSII design using fully open-source toolchains.
The new SG13CMOS5L variant offers an economical MPW option based on a reduced BEOL stack, lowering fabrication cost and turnaround time while maintaining compatibility with established open-source design flows and verification infrastructure.
Analog and RF design support continues to mature with ongoing gnucap integration and model validation efforts, strengthening open-source circuit simulation capabilities. Qucs-S support has been enhanced through XML-based symbol definitions, improving schematic consistency and maintainability within open design environments.
PDK robustness has been further increased through continuous DRC and LVS rule deck refinements, improving verification reliability and cross-tool consistency. In parallel, the device portfolio has expanded with the integration of LDMOS devices for power and high-voltage applications, as well as emerging ReRAM capabilities, broadening the technology's applicability to advanced mixed-signal and memory-oriented research designs.

14:30 – 15:00: Lecture 6

An Overview of Fault Injection Techniques for Neural Network Accelerators

Rizwan Tariq Syed, IHP, Frankfurt (Oder), Germany

Bio: Rizwan Tariq Syed received a Master of Science in Communication Engineering degree from the Technical University of Munich, Germany. In 2025, he received a PhD degree from the University of Potsdam and is currently associated with IHP as a research scientist. For the last few years, his work has been mainly focused on fault-tolerant and reconfigurable AI accelerators on FPGAs. At IHP, He has been involved in many research and development projects such as EMPHASE, Space Region, Open6G Hub, and TAICHIP.

Abstract: Artificial Intelligence has been an integral part of a wide range of applications. Its impact goes beyond traditional image processing and extends toward safety critical domains such as automotive, medical, and space applications. Thus, in order to ensure the system works correctly under the influence of faults, the fault injection (FI) technique is often utilized. In recent years, the complexity of AI processing systems has grown. Thus, in order to understand how these complex processing systems behave under faults, a single FI methodology may not be enough. This study broadly classifies FI methods into four methodologies, i.e., software-based FI(SWFI), simulation-based FI (SFI), hardware-based FI(HWFI), and emulation-based FI (EFI). Additionally, this study discusses the impact of faults in deep neural networks (DNNs) and the working principles, tools, and pros/cons of various fault injection methodologies.

Wednesday, 13th May

11:00 – 11:45: Keynote Talk 4

When Hardware Fails, Does Intelligence Survive? Faults in Neuromorphic Communication Hardware

Davide Bertozzi, University of Manchester, Manchester, UK

Bio: Davide Bertozzi is a Reader in Advanced Processing Technologies at University of Manchester (United Kingdom). He got his PhD at University of Bologna (Italy) in 2003 and led the multiprocessor system-on-chip group at University of Ferrara till 2023. The mission of his research is to stay at the forefront of system innovation by leveraging the enabling properties of interconnection architectures and emerging technologies. He has been visiting researcher at Stanford University and at several semiconductor industries (STMicroelectronics, NEC America Labs, NXP, Samsung). In 2018 he received the Wolfgang Mehr Award from IHP Microelectronics, a Leibniz Institute for innovative microelectronics in Germany, for his interdisciplinary research on photonically-integrated systems. His research interests span widely across the field of on-chip communication with a strong drive to overcome the communication bottleneck in emerging system architectures, ranging from neuromorphic computing to multi-tenant fog nodes.
He currently contributes to the activities for neuroscience simulation acceleration within the flagship EBRAINS 2.0 project, and takes part to a collaborative effort to bring the celebrated SpiNNaker large-scale neuromorphic computing platform to the next generations of technology, implementation and architecture. Finally, he is deeply involved in recent EU-funded initiatives (TAICHIP, TWIN-RELECT, AIDA4Edge) to enhance networking between research institutions of the widening countries and top-class leading counterparts, encompassing joint research, knowledge transfer and exchange of best practices in the fields of AI chips, open EDA tools and hybrid SNN-ANN models, respectively. His scientific activity has led to roughly 200 publications, with five best paper awards, three best paper award nominations and one high-impact paper award for one of the five most cited papers in the first thirty years of the Int. Conference of Computer Design.

Abstract: Neuromorphic computers aim to mimic the brain by exchanging information through discrete electrical “spikes,” much like neurons do. In these systems, intelligence does not emerge only from computation inside artificial neurons, but also from the reliable communication of spikes across the chip. But what happens when this communication infrastructure starts to degrade? Most reliability studies so far have focused on faults inside neurons or memory elements. In this work, the perspective shifts to a less explored question: how sensitive is intelligent behavior to permanent faults in the hardware that routes spikes between different parts of the system? For this purpose, a cross-layer simulation framework is developed that connects detailed hardware-level fault models with high-level spiking neural network simulations. This allows to trace how low-level defects, such as signals getting lost, duplicated, or misdirected, propagate upward and affect task performance. The results highlight a fundamental point: in neuromorphic systems, intelligence is not only about neurons and learning algorithms,

but it critically depends on the physical reliability of the communication substrate that binds them together.

12:15 – 13:00: Lecture 7

Considerations on the Mixed-Criticality Task Execution in Multicore Architecture for Real-Time Applications

Fabian Vargas, IHP, Frankfurt (Oder), Germany

Bio: Fabian Vargas obtained the Ph.D. Degree in Microelectronics from the Institut National Polytechnique de Grenoble (INPG), France, in 1995. At present, he is Senior Scientist at IHP - Leibniz Institute for High Performance Microelectronics, Germany, where he works on on-chip sensors and cross-layer resilience for aerospace-application systems. Fabian Vargas has served as Technical Committee Member and Guest-Editor in many IEEE-sponsored conferences and journals. He holds several patents and published over 200 refereed papers. Fabian Vargas was researcher of the BR National Science Foundation from 1996 to 2023. He co-founded the IEEE-Computer Society Latin American Test Technology Technical Council (IEEE LA-TTTC) in 1997 and the IEEE Latin American Test Symposium (LATS) in 2000. He received the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of these groups. Fabian Vargas is Golden Core Member of the IEEE Computer Society and Senior Member of the IEEE.

Abstract: The use of multicore processors in general-purpose real-time embedded systems has experienced a huge increase in recent years. Unfortunately, critical applications are not benefiting from this type of processors as one could expect. The major obstacle is that we may not predict and provide any guarantee on real-time properties of software running on such platforms. The shared memory bus is among the most critical resources, which severely degrades the timing predictability of multicore software due to the bus access contention between cores. This talk discusses the applicability of hardware-based approaches to support mixed-criticality workload execution in a multicore processor-based embedded system. The basic idea is to allow any number of cores to run less-critical tasks concurrently with the critical core, which is running the critical task. These approaches are based on the use of an infrastructure intellectual property (I-IP) core, implemented in hardware, which allows the execution of any number of cores (running less-critical workloads) concurrently with the critical core (executing the critical workload). This capacity allows the exploitation of the maximum performance offered by a multiprocessing system while guaranteeing critical task schedulability, i.e., that the critical task execution will not violate timing deadline. A case-study based on a dual-core version of the LEON3 softcore processor was implemented in VHDL language. Practical experiments demonstrate the effectiveness of these ideas on combining system high performance with critical task schedulability within timing deadline.

14:00 – 14:30: Lecture 8
Commercialization of Academic Research Results
Anders Henriksson, IHP Solutions, Frankfurt (Oder), Germany

Bio: Anders Henriksson is a researcher and technology transfer professional with a background in materials science and bioelectronics. He has conducted research at several institutions including the University of Vienna, the University of Tokyo, and TU Berlin. Currently, he serves as IP Coordinator and Technology Transfer Manager at IHP Solutions, where he focuses on the commercialization of advanced semiconductor technologies developed at IHP.

Abstract: This presentation discusses how academic research in microelectronics can be translated into industrial impact and how technology transfer can be actively enabled. It introduces typical commercialization pathways in semiconductor research, with a focus on reusable circuit IP and collaborative development. Using examples from our latest transfer projects, the talk illustrates how we work to support the transition from research results to industrial applications and highlights practical considerations for researchers who aim to make their work relevant beyond academia.

14:30 – 15:00: Lecture 9
Preparing Project Proposals
Milos Krstic, IHP, Frankfurt (Oder), Germany

Bio: Milos Krstic received the Dr-Ing. degree in electronics from Brandenburg University of Technology, Cottbus, Germany in 2006. Since 2001 he has been with IHP, Frankfurt (Oder), Germany, where he leads the department System Architectures. From 2016 he is also professor for “Design and Test Methodology” at the University of Potsdam. For the last few years, his work was mainly focused on fault tolerant architectures and design methodologies for digital systems integration. Prof. Krstic has been managing many international and national R&D projects. He is also leading and coordinating space activities at IHP. He has published more than 250 journal and conference papers, and registered 12 patents.

Abstract: In this talk, the existing funding programs at the national and international level will be explained. The strategy for consortium assembling and project basic conception will be derived. The process of project proposal preparation will be discussed in detail, and major pitfalls will be elaborated.